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VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2827	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/006,292	PATEL ET AL.
	Examiner	Art Unit
	John B. Vigushin	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *16-30 and 65-99* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *88-99* is/are allowed.

6)☒ Claim(s) *16-24,26-30,65-78,81,82,84 and 85* is/are rejected.

7)☒ Claim(s) *25,79,80,83,86 and 87* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Claims 16-30 in the instant Amendment (Paper No. 1203) is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 22 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 22 and 27 each recite "the at least one conductor" in line 2. The antecedent basis for this limitation is unclear. Does it reference the "at least one of the conductors" of the "plurality of conductors" in base Claim 16, or, does it reference the specific conductor or conductors to which the capacitor is electrically coupled?

Rejections Based On Prior Art

4. The following references were relied upon for the rejections hereinbelow:

Menzies, Jr. et al. (US 4,882,656)

Baudouin et al. (US 6,040,983)

Tao et al. (US 6,316,828 B1)

Galvagni et al. (US 6,459,561 B1)

Wallace (US 5,010,447)

Salem (US 6,300,677 B1)

Drake et al. (US 6,404,649 B1)

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 16, 17, 22-24, 28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Drake et al.

As to Claim 16, Drake et al. discloses, in Figs. 2 and 3: a substrate 101 having a plurality of conductors 104 and 105 within an IC mounting region; at least one capacitor 103 within the IC mounting region and electrically coupled to at least one of the conductors (i.e., conductors 104; col.3: 45-48); and an IC 110 electrically coupled to the plurality of conductors 104 and 105.

As to Claim 17, Drake et al. further discloses the at least one capacitor 103 is electrically coupled to first and second conductors 104 of the plurality of conductors 104 and 105, and wherein the first conductor couples to a first potential, and the second conductor couples to a second potential (col.3: 49-51).

As to Claim 22 (as best understood in view of the 35 USC § 112, 2nd paragraph rejection set forth, above), Drake et al. further discloses the at least one capacitor 103 is

mounted beside the at least one conductor 104 (Figs. 2 and 5A,B; the metallized castellations 1031 are mounted beside the conductors 104, then connected thereto by solder; col.3: 51-53).

As to Claim 23, Drake et al. further discloses the at least one capacitor 103 is mounted between two conductors 104 (Fig. 2).

As to Claim 24, Drake et al. further discloses, in Figs. 5A,B, the at least one capacitor 103 has terminal 1033 on its top side, terminals 1034 and 1035 on its bottom side and terminals 1031 on its opposing sides.

As to Claim 28, Drake et al. further discloses, in Fig. 2, a plurality of capacitors 103 distributed substantially throughout the IC mounting region, each capacitor 103 being in electrical contact with at least one of the conductors 104.

As to Claim 30, Drake further discloses, in Fig. 2, that conductors 104 and 105 include pads (col.3: 45-48).

7. Claims 16-19, 22, 23 and 26 are rejected under 35 U.S.C. 102(b) as being anticipated by Menzies, Jr. et al.

As to Claim 16, Menzies, Jr. et al. discloses, in Fig. 1, a substrate 12 having a plurality of conductors 16a-x and 17a-x within an IC mounting region; at least one capacitor 20 within the IC mounting region and electrically coupled to at least one of the conductors (i.e., coupled to conductors 16x and 17a); an IC 11 electrically coupled to the plurality of conductors 16a-x and 17a-x (col.3: 55-col.4: 26).

As to Claim 17, Menzies, Jr. et al. further discloses the at least one capacitor 20 is electrically coupled to first and second conductors 16x and 17a, wherein first

conductor 16x is coupled to a first potential and second conductor 17a is coupled to a second potential (Figs. 1 and 2; col.4: 7-33).

As to Claim 18, Menzies, Jr. et al. further discloses the at least one capacitor 20 is mounted atop the at least one conductor 16x (Figs. 1 and 3; tabs 31 and 32 of capacitor 20 have trace ends 35 and 39, respectively. Tab 31 of capacitor 20 is mounted atop the at least one conductor 16x).

As to Claim 19, Menzies, Jr. et al. further discloses the at least one capacitor 20 is mounted atop the at least one conductor 16x (Figs. 1 and 3; tabs 31 and 32 of capacitor 20 have trace ends 35 and 39, respectively. Tabs 31 and 32 of capacitor 20 are mounted atop two conductors 16x and 17a, respectively).

As to Claim 22 (as best understood in view of the 35 USC § 112, 2nd paragraph rejection set forth, above), Menzies, Jr. et al. further discloses the at least one capacitor 20 is mounted beside the at least one conductor; i.e., mounted beside all the conductors 16 and 17 except a to 16x and 17a (Fig. 1).

As to Claim 23, Menzies, Jr. et al. further discloses the at least one capacitor 20 is mounted between two conductors; i.e., between any one of conductors 16 (except 16x) adjacent one edge of capacitor 20 and any one of conductors 17 (except 17a) adjacent the opposite edge of capacitor 20 (Fig. 1).

As to Claim 26, Menzies, Jr. et al. further discloses the plurality of conductors are substantially parallel to one another; i.e., conductors 16a-x form an array substantially parallel to the array formed of conductors 17a-x.

8. Claims 16-19, 22-24, 26 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Wallace.

As to Claim 16, Wallace discloses, in Figs. 1 and 3, a substrate 12 having a plurality of conductors 20, 52, 54, 62, 64 within an IC mounting region; at least one capacitor 16 within the IC mounting region and electrically coupled to at least one of the conductors 20, 52, 54, 62 and 64; and an IC 14 electrically coupled to the plurality of conductors.

As to Claim 17, Wallace further discloses the at least one capacitor 16 is electrically coupled to first and second conductors 52 and 62, respectively, and the first conductor is coupled to a first potential Vdd and the second conductor is coupled to a second potential Vss (Fig. 3).

As to Claim 18, Wallace further discloses the at least one capacitor 16 is mounted atop the at least one conductor 52 (Fig. 3).

As to Claim 19, Wallace further discloses the at least one capacitor 16 is mounted atop two conductors 52 and 62 (Fig. 3).

As to Claim 22 (as best understood in view of the 35 USC § 112, 2nd paragraph rejection set forth, above), Wallace further discloses the at least one capacitor 16 is mounted beside the at least one conductor 20 of the plurality of conductors.

As to Claim 23, Wallace further discloses the at least one capacitor 16 is mounted between two conductors 20.

As to Claim 24, Wallace further discloses the at least one capacitor 16 has a top, bottom and a pair of opposing sides, and has terminals 40 and 42 on its opposing sides (Fig. 3).

As to Claim 26, Wallace further discloses, in Figs. 1 and 2, a substrate 12 having a plurality of conductors 20, 28 and 36 within an IC mounting region; at least one capacitor 16 within the IC mounting region and electrically coupled to at least one of the conductors (i.e., conductors 28 and 36); and an IC 14 electrically coupled to the plurality of conductors 20, 28 and 36; the plurality of conductors 28 and 36 are substantially parallel to one another.

As to Claim 30, Wallace further discloses that conductors 20, 52, 54, 62 and 64 include pads (Fig. 3; col.3: 39-40; col.4: 25-28 and 47-49).

9. Claims 16-19, 22-24, 26-28 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Tao et al.

As to Claim 16, Tao et al. discloses, in Figs. 5 and 6, a substrate 300 having a plurality of conductors 301, 302 and 304 [*Examiner's Note*: element 304 is called an "opening" but the "opening" has a pad and therefore, element 304 will be considered a conductor; see col.3: 34-36] within an IC mounting region; at least one capacitor 311 within the IC mounting region and electrically coupled to at least one of the conductors (col.3: 23-24, 34-36 and 44-48); an IC coupled to the plurality of conductors.

As to Claim 17, Tao et al. further discloses at least one capacitor 311 is electrically coupled to first and second conductors 304, wherein the first conductor is

coupled to a first potential and the second conductor is coupled to a second potential (col.3: 23-24 and 44-48).

As to Claim 18, Tao et al. further discloses at least one capacitor 311 is mounted atop the at least one conductor 304 (Figs. 5 and 6).

As to Claim 19, Tao et al. further discloses the at least one capacitor 311 is mounted atop two conductors 304 (Figs. 5 and 6).

As to Claim 22 (as best understood in view of the 35 USC § 112, 2nd paragraph rejection set forth, above), Tao et al. further discloses the at least one capacitor 311 is mounted beside the at least one conductor 301 and 302 (Fig. 6).

As to Claim 23, Tao et al. further discloses the at least one capacitor 16 is mounted between two conductors 301 and 302 (Fig. 6).

As to Claim 24, Tao et al. further discloses the at least one capacitor 311 has a top, bottom, and a pair of opposing sides, and the at least one capacitor 311 has terminals on its opposing sides (Figs. 1 and 6).

As to Claim 26, Tao et al. further discloses that the plurality of conductors 301, 302 and 304 are substantially parallel to one another (conductors 301 and 302 are substantially parallel to one another and conductor pads 304 are respectively collinear with parallel conductors 301 and 302).

As to Claim 27 (as best understood in view of the 35 USC § 112, 2nd paragraph rejection set forth, above), Tao et al. further discloses the at least one capacitor 311 is non-orthogonally mounted atop the at least one conductor (Fig. 6).

As to Claim 28, Tao et al. further discloses a plurality of capacitors 311 distributed substantially throughout the IC mounting region, each capacitor 311 being in electrical contact with at least one of the conductors 304.

As to Claim 30, Tao et al. further discloses conductors 304 include pads (col.3: 34-36).

10. Claims 16-21, 24, 26, 28, 29, 65-73, 75-78, 81, 82, 84 and 85 are rejected under 35 U.S.C. 102(e) as being anticipated by Salem.

As to Claim 16, Salem discloses, in Figs. 2 and 4A,B,C: a substrate 84 having a plurality of conductors (not shown, but on the top surface and the conductive well for electrically connecting the IC 82 and capacitor 86 assembly; col.4: 10-30); within an IC mounting region; at least one capacitor 86 within the IC mounting region and electrically coupled to at least one of the conductors (col.4: 10-30); IC 82 electrically coupled to the plurality of conductors (col.4: 10-30).

As to Claim 17, Salem further discloses the at least one capacitor 86 is electrically coupled to first and second conductors in connection well 88, and wherein the first conductor is coupled to a first potential and the second conductor is coupled to a second potential in accordance with the structure of at least one capacitor 86 (Figs. 2 and 4A,B,C; col.3: 40-65 wherein the described capacitor 40 is structurally analogous to the capacitor 86).

As to Claim 18, Salem further discloses the at least one capacitor 86 is mounted atop the at least one conductor (Fig. 4A; col.4: 10-30).

As to Claim 19, Salem further discloses the at least one capacitor 86 is mounted atop two conductors (Figs. 2 and 4A; col.3: 40-65 and col.4: 10-30).

As to Claim 20, Salem further discloses that the at least one capacitor 86 in Fig. 4A (40 in Fig. 2) is a capacitor array having two surfaces, each surface having a plurality of terminals of first and second polarity types. For example, in Fig. 2, the first capacitor of capacitor array 40 may be formed of metal sections 42 and 44, wherein the top and bottom surfaces of capacitor section 42 are at a positive polarity and the top and bottom surfaces of capacitor section 44 are at a negative polarity, and similarly for sections 46 and 48 of the second capacitor of capacitor array 40 (col.3: 8-15 and 44-51).

As to Claim 21, Salem further discloses the plurality of terminals are disposed over substantially the entire surfaces (sections 42, 44, 46 and 48 are each metal sections and top portions 54, bottom portions 56 and the side portions are all continuous metal terminals with sites 50 and 52 for surface mount bump connections (col.2: 58-col.3: 15).

As to Claim 24, Salem further discloses the at least one capacitor 86 in Fig. 4A (40 in Fig. 2) has terminals on its top, bottom, and opposing sides (Fig. 2; col.2: 58-col.3: 15).

As to Claim 26, Salem further discloses the plurality of conductors (of substrate 84) are substantially parallel to one another (this is inherently so due to the disclosed terminal configuration of the IC 82 and the assembly of capacitor arrays 86 (Figs. 4A,B,C).

As to Claim 28, Salem further discloses a plurality of capacitors 86 distributed substantially throughout the IC mounting region, each capacitor 86 being in electrical contact with at least one of the conductors of substrate 84.

As to Claim 29, Salem further discloses the plurality of capacitors 86 comprises a plurality of sets of capacitors: For example, capacitor 86 is a larger embodiment of similar capacitor 40 (col.3: 10-15), wherein capacitor 40 comprises a set of two capacitors, the first capacitor formed of metal sections 42, 44 and the second capacitor formed of metal sections 46, 48. There are a plurality of such capacitors 86 that each are formed of a set of four capacitors--each formed of two metal sections just like capacitor 40--as shown in Fig. 4C. Each capacitor set 86 comprising the four capacitors aligned substantially end-to-end (compare Figs. 2 and 4C).

As to Claim 65, Salem discloses, in Figs. 2 and 4A,B,C: a substrate 84 having a plurality of conductors within an IC mounting region; at least one capacitor 86 within the IC mounting region and electrically coupled to at least one of the conductors, wherein the at least one capacitor 86 is mounted atop the at least one conductor (by way of solder bumps); an IC 82 electrically coupled to the plurality of conductors via the at least one capacitor 86 (col.4: 10-30).

As to Claim 66, Salem further discloses the at least one capacitor 86 is electrically coupled to first and second conductors--in connection well 88--of the plurality of conductors, and wherein the first conductor is coupled to a first potential and the second conductor is coupled to a second potential in accordance with the structure of at

least one capacitor 86 (Figs. 2 and 4A,B,C; col.3: 40-65 wherein the described capacitor 40 is structurally analogous to the capacitor 86).

As to Claim 67, Salem further discloses the at least one capacitor 86 has a top and a bottom, and wherein the at least one capacitor 86 has terminals on its top and bottom (Figs. 2 and 4A; col.4: 10-30).

As to Claim 68, Salem further discloses a plurality of capacitors 86 distributed substantially throughout the IC mounting region, each capacitor 86 being in electrical contact with at least one of the conductors (Figs. 4A,B).

As to Claim 69, Salem further discloses the plurality of capacitors 86 comprises a plurality of sets of capacitors: For example, capacitor 86 is a larger embodiment of similar capacitor 40 (col.3: 10-15), wherein capacitor 40 comprises a set of two capacitors, the first capacitor formed of metal sections 42, 44 and the second capacitor formed of metal sections 46, 48. There are a plurality of such capacitors 86 that each are formed of a set of four capacitors--each formed of two metal sections just like capacitor 40--as shown in Fig. 4C. Each capacitor set 86 comprising the four capacitors aligned substantially end-to-end (compare Figs. 2 and 4C).

As to Claim 70, Salem discloses, in Figs. 2 and 4A,B,C: a substrate 84 having a plurality of conductors within an IC mounting region; a plurality of capacitors 86 distributed substantially throughout the IC mounting region and electrically coupled to at least one of the conductors, wherein the plurality of capacitors 86 comprises a plurality of capacitor arrays (each capacitor 86 in Figs. 4A,B,C is a capacitor array of the type in

Fig. 2; see col.3: 8-57); an IC 82 electrically coupled to the plurality of conductors via the plurality of capacitors 86 (col.4: 10-30).

As to Claim 71, Salem further discloses that selected ones of the plurality of capacitors 86 are electrically coupled to first and second conductors in connection well 88, and wherein the first conductor is coupled to a first potential and the second conductor is coupled to a second potential in accordance with the structure of capacitors 86 (Figs. 2 and 4A,B,C; col.3: 40-65 wherein the described capacitor 40 is structurally analogous to each of capacitors 86).

As to Claim 72, Salem further discloses each of the plurality of capacitors has a top and a bottom, and wherein selected ones of the plurality of capacitors 86 have at least one terminal on their top and at least one terminal on their bottom (compare Figs. 2 and 4A; col.4: 10-30).

As to Claim 73, Salem further discloses each of the capacitor arrays has a top and a bottom, and wherein selected ones of the capacitor arrays have a plurality of terminals of first and second polarities on their top and a plurality of terminals of first and second polarities on their bottom (compare Figs. 2 and 4A,B,C; note that in exemplary capacitor array 40 of Fig. 2, metal sections 42 and 44 form a capacitor and the top and bottom of section 42 are positive while the top and bottom of section 44 are negative; similarly for the capacitor formed of metal sections 46 and 48; see col.3: 40-57).

As to Claim 75, Salem discloses, in Figs. 2 and 4A,B,C: a substrate 84 having a plurality of conductors within an IC mounting region, wherein the plurality of conductors are substantially parallel to one another (this is inherently so due to the disclosed

terminal configuration of the IC 82 and the assembly of capacitor arrays 86 (Figs. 4A,B,C); a plurality of capacitors 86 within the IC mounting region and electrically coupled to at least one of the conductors, wherein the plurality of capacitors 86 comprises a plurality of capacitor arrays (each capacitor 86 in Figs. 4A,B,C is a capacitor array of the type in Fig. 2; see col.3: 8-57); an IC 82 electrically coupled to the plurality of conductors via the plurality of capacitors 86 (col.4: 10-30).

As to Claim 76, Salem further discloses that selected ones of the plurality of capacitors 86 are electrically coupled to first and second conductors in connection well 88, and wherein the first conductor is coupled to a first potential and the second conductor is coupled to a second potential in accordance with the structure of capacitors 86 (Figs. 2 and 4A,B,C; col.3: 40-65 wherein the described capacitor 40 is structurally analogous to each of capacitors 86).

As to Claim 77, Salem further discloses each of the plurality of capacitors has a top and a bottom, and wherein selected ones of the plurality of capacitors 86 have at least one terminal on their top and at least one terminal on their bottom (compare Figs. 2 and 4A; col.4: 10-30).

As to Claim 78, Salem further discloses each of the capacitor arrays has a top and a bottom, and wherein selected ones of the capacitor arrays have a plurality of terminals of first and second polarities on their top and a plurality of terminals of first and second polarities on their bottom (compare Figs. 2 and 4A,B,C; note that in exemplary capacitor array 40 of Fig. 2, metal sections 42 and 44 form a capacitor and the top and

bottom of section 42 are positive while the top and bottom of section 44 are negative; similarly for the capacitor formed of metal sections 46 and 48; see col.3: 40-57).

As to Claim 81, Salem discloses, in Figs. 2 and 4A,B,C: a substrate 84 having a plurality of conductors within an IC mounting region; a capacitor array 86 in Figs. 4A,B,C (similar to the capacitor array 40 of Fig. 2; col.3: 40-57) within the IC mounting region and electrically coupled to at least one of the conductors; and an IC 82 electrically coupled to the plurality of conductors via the capacitor array 86 (col.4: 10-30).

As to Claim 82, Salem further discloses the capacitor array 86 is electrically coupled to first and second conductors--in connection well 88--of the plurality of conductors, and wherein the first conductor is coupled to a first potential and the second conductor is coupled to a second potential in accordance with the structure of at least one capacitor 86 (Figs. 2 and 4A,B,C; col.3: 40-65 wherein the described capacitor 40 is structurally analogous to the capacitor 86).

As to Claim 84, Salem further discloses the capacitor array 86 has a top and a bottom, and wherein the capacitor array 86 has at least one terminal on its top and at least one terminal on its bottom (compare Figs. 2 and 4A; col.4: 10-30).

As to Claim 85, Salem further discloses the capacitor array has a plurality of terminals of first and second polarities on its top and a plurality of terminals of first and second polarities on its bottom (compare Figs. 2 and 4A,B,C; note that in exemplary capacitor array 40 of Fig. 2, metal sections 42 and 44 form a capacitor and the top and

bottom of section 42 are positive while the top and bottom of section 44 are negative; similarly for the capacitor formed of metal sections 46 and 48; see col.3: 40-57).

11. Claims 65, 67 and 68 are rejected under 35 U.S.C. 102(b) as being anticipated by Baudouin et al.

As to Claim 65, Baudouin et al. discloses, in Figs. 3 and 4: a substrate 16 having a plurality of conductors 16b within an IC mounting region (col.3: 49-col.4: 3); at least one capacitor 20 (col.3: 31-33) within the IC mounting region and electrically coupled to at least one of the conductors 16b, wherein the at least one capacitor is mounted atop the at least one conductor 16b; an IC 18 electrically coupled to the plurality of conductors 16b via the at least one capacitor 20.

As to Claim 67, Baudouin et al. further discloses the at least one capacitor 20 has terminals on its top and bottom (Fig. 3).

As to Claim 68, Baudouin et al. further discloses a plurality of capacitors 20 distributed substantially throughout the IC mounting region, each capacitor being in electrical contact with at least one of the conductors 16b (col.1: 33-35; col.3: 49-col.4: 3).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

14. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Salem.

Salem discloses the surface mounting of IC 82 and capacitors 86 on substrate 84 but does not explicitly depict or describe the substrate conductors that receive the IC and capacitor solder bumps and thereby effectively surface mount and electrically couple the IC 82 and capacitors 86 to the substrate 84. However, the use of pads for receiving solder bumps is notorious in the art of surface mounting components and would have been obvious to one ordinary skill in the art at the time the invention was made for the purpose of effecting a mechanically and electrically reliable connection of the components to the substrate.

15. Claim 74 is rejected under 35 U.S.C. 103(a) as being unpatentable over Salem in view of Galvagni et al.

I. Salem discloses capacitors 86 in Figs. 4A,B,C of the type similar to capacitor 40 in Fig. 2 and described in detail in col.3: 40-65. Salem also discloses that different

types of capacitors could also be used and gives only one example corresponding to Appln. 09/320,241, now US 6,252,760 (col.4: 35-40).

II. Galvagni et al. discloses an interdigitated capacitor 20 that is a capacitor array (Fig. 4B; col.9: 8-13) assembled with solder balls 24 for surface mounting (col.8: 47-49).

III. Since Salem and Galvagni et al. disclose capacitor arrays mounted on a substrate and Salem teaches various polarity schemes for the capacitor arrays in col.3: 40-650 and teaches various types of capacitors for effecting those required polarity schemes in col.4: 35-40, then the use of the interdigitated capacitor structure of the capacitor array in Galvagni et al. would have been readily recognized in the pertinent art of Salem for joining a chip having an electrical layout and structure requiring such a capacitor array to the substrate.

IV. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the capacitor array structure of Salem with the interdigitated capacitor array structure of Galvagni et al. in order to join a chip to a substrate via a capacitor array having a polarity arrangement suited to the electrical layout of the chip and substrate package.

Allowable Subject Matter

16. Claims 88-99 have been allowed.

17. Claims 25, 79-80, 83 and 86-87 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

18. The following is a statement of reasons for the indication of allowable subject matter:

As to Claim 25, patentability resides in the limitation wherein *the conductors include at least one conductive bar having a height and a width, the height exceeding the width*, in combination with the other limitations of the claim.

As to Claims 79-80, patentability resides in the limitation wherein *the plurality of capacitor arrays are non-orthogonally mounted atop the plurality of conductors*, in combination with the other limitations of the broadest claim, Claim 79.

As to Claim 83, patentability resides in the limitation wherein *the capacitor array is non-orthogonally mounted atop the plurality of conductors*, in combination with the other limitations of the claim.

As to Claims 86-87, patentability resides in the limitation wherein *the plurality of conductors comprise at least first and second conductive bars having a height and a width, the height exceeding the width*, in combination with the other limitations of the broadest claim, Claim 86.

As to Claims 88-96, patentability resides in the limitation wherein *the conductors include at least one conductive bar having a height and a width, the height exceeding the width*, in combination with the other limitations of base Claim 88.

As to Claims 97-99, patentability resides in *the conductive bars having a height and a width, the height exceeding the width*, in combination with the other limitations of base Claim 97.

19. As allowable subject matter has been indicated, applicant's reply must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 CFR 1.111(b) and MPEP § 707.07(a).

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) The following references disclose integrated circuits mounted to substrates via capacitors:

Kudoh et al. (US 6,373,714 B1): Figs. 3A,B,C.

Yoon (US 6,320,249 B1): Figs. 2 and 3.

Farooq et al. (US 6,178,082 B1): Figs. 1 and 2; capacitor 13.

Hernandez (US 5,272,590): Figs. 15 and 18.

b) The following references disclose a capacitor mounted within an IC mounting region:

Yamaguchi et al. (US 6,147,876): Fig. 24: capacitor 134; col.14: 40-42.

Goodwin et al. (US 6,043,987): Figs. 3-6.

Chu et al. (US 5,996,880): Fig. 6; col.7: 53-65.

Oh et al. (US 5,504,373): Figs. 4A and 5; col.5: 31-36.

Johnson (US 4,879,631): Figs. 1 and 2.

c) Sen (US 6,252,760 B1) discloses a capacitor 40 cited in Salem (US 6,300,677 B1; col.4: 35-40). Salem was relied upon for some of the art rejections set forth, above, including the rejection of Applicant's Claim 74.

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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jbv
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